

1        1.    A computer system comprising:  
2        a hierarchical memory system, including a first local  
3 storage, and a main storage; and  
4        a first memory access unit coupled to the hierarchical  
5 memory system capable of processing a plurality of memory  
6 access instructions that includes  
7        (a) a first instruction that specifies a first address  
8 and a first value, wherein processing the first instruction  
9 by the first memory access unit causes the first value to  
10 be stored at a location in the first local storage that is  
11 associated with the first address, and  
12        (b) a second instruction that specifies the first  
13 address, wherein processing of the second instruction by  
14 the first memory access unit after processing the first  
15 instruction is such that the first memory access unit  
16 complete processing of the second instruction after the  
17 first value is stored at a location in the main storage  
18 that is associated with the first address.

1           2.    The computer system of claim 1 wherein the  
2 plurality of memory access instructions further includes  
3           (c) a third instruction that specifies the first  
4 address, wherein processing of the third instruction by the  
5 first memory access unit causes a value to be retrieved  
6 from a location in the first local storage that is  
7 associated with the first address, and  
8           (d) a fourth instruction that specifies the first  
9 address, wherein processing of the fourth instruction by  
10 the first memory access unit prior to processing the third  
11 instruction causes the value retrieved during processing  
12 the third instruction to be a value that was retrieved from  
13 a location in the main storage that is associated with the  
14 first address at a time after the fourth instruction was  
15 begun to be processed.

1           3.    The computer system of claim 1 wherein the  
2 hierarchical memory system further includes a second local  
3 storage, and the computer system further comprises a second  
4 memory access unit coupled to the hierarchical memory  
5 system capable of processing the plurality of memory  
6 access, and the plurality of instructions further includes:

7           (c) a third instruction that specifies the first  
8 address, wherein processing of the third instruction by the  
9 second memory access unit causes a value to be retrieved  
10 from a location in the second local storage that is  
11 associated with the first address, and

12           (d) a fourth instruction that specifies the first  
13 address, wherein processing of the fourth instruction by  
14 the second memory access unit prior to processing the third  
15 instruction and after the first memory access unit has  
16 completed processing the second instruction causes the  
17 value retrieved during processing the third instruction to  
18 be a value that was retrieved from a location in the main  
19 storage that is associated with the first address at a time  
20 after the fourth instruction was begun to be processed,  
21 whereby the value caused to be retrieved by the processing  
22 of the third instruction by the second memory access unit  
23 is the first value, which was specified in the first  
24 instruction which was processed by the first memory access  
25 unit.

1        4.    A computer processor for use in a multiple  
2 processor system in which the computer processor is coupled  
3 to one or more other processors through a memory system,  
4 the computer processor comprises a memory access unit  
5 configured to access the memory system by processing a  
6 plurality of memory access instructions, including  
7        (a) a first instruction that specifies a first address  
8 and a first value, wherein processing the first instruction  
9 causes the first value to be stored at a location in the  
10 memory system that is associated with the first address,  
11 such that for at least some period of time the one or more  
12 other processors do not have access to the first value, and  
13        (b) a second instruction that specifies the first  
14 address, wherein processing of the second instruction after  
15 processing the first instruction is such that the  
16 processing of the second instruction completes after the  
17 first value is accessible to each of the one or more other  
18 processors.

1        5. The computer processor of claim 4 wherein the  
2 plurality of memory access instructions further includes  
3        (c) a third instruction that specifies a second  
4 address, wherein processing of the third instruction causes  
5 a value to be retrieved from a location in the memory  
6 system that is associated with the second address, and  
7        (d) a fourth instruction that specifies the second  
8 address, wherein processing of the fourth instruction prior  
9 to processing the third instruction causes the third  
10 instruction to retrieve a value that was previously stored  
11 in the memory system by one of the one or more other  
12 processors.

1        6. A multiple processor computer configured to use a  
2 storage system, the computer comprising a plurality of  
3 memory access units, including:  
4        a first memory access unit responsive to execution  
5 of instructions by a first instruction processor, wherein  
6 the first memory access unit is coupled to the storage  
7 system; and  
8        a second memory access unit responsive to execution  
9 of instructions by a second instruction processor, wherein  
10 the second memory access is coupled to the storage system;  
11        wherein the first and the second memory access units  
12 are each capable of issuing memory access messages to the  
13 storage system and receiving return messages from the  
14 storage system in response to the memory access messages,  
15 the memory access messages and return messages including:  
16        a first memory access message that specifies a first  
17 address and a first value for causing the first value to be

18 stored at a first location in storage system that is  
19 associated with the first address;

20 a first return message that is a response to the  
21 first memory access message, indicating that the first  
22 value has been stored in the storage system at a location  
23 that is associated with the first address and that is  
24 accessible to the memory access unit receiving the first  
25 return message;

26 a second return message indicating that the first  
27 value has been stored in the storage system at a location  
28 that is associated with the first address and that is  
29 accessible to each of the plurality of memory access units.

1 7. The multiple processor computer of claim 6  
2 wherein the memory access messages and return messages  
3 further include a second memory access message that  
4 specifies the first address, and wherein the second return  
5 message is a response to the second memory access message.

1 8. The multiple processor computer of claim 7 wherein  
2 the first memory access unit is configured to issue the  
3 first memory access message in response to execution of a  
4 first processor instruction that specifies the first  
5 address and the first value, and is configured to issue the  
6 second memory access message in response to execution of a  
7 second processor instruction that specifies the first  
8 address.

1           9.   A memory system for use in a multiple processor  
2 computer system in which the memory system is coupled to a  
3 plurality of computer processors, wherein the memory system  
4 comprises a plurality of local storages, including a first  
5 local storage unit and other local storage units, and each  
6 local storage unit is capable of processing a plurality  
7 messages received from a corresponding one of the computer  
8 processors, the plurality of messages includes:  
9           (a) a first message that specifies a first address and  
10 a first value, wherein processing the first message by the  
11 first local storage unit causes the first value to be  
12 stored at a location in the local storage unit that is  
13 associated with the first address, such that, for at least  
14 a period of time, the other local storage units do not have  
15 access to the first value, and  
16           (b) a second message that specifies the first address,  
17 wherein processing of the second message by the first local  
18 storage unit after processing the first message is such  
19 that the processing of the second message completes after  
20 the first value can be accessed by each of the other local  
21 storage units.

1        10. The memory system of claim 9 wherein the  
2 plurality of memory access messages further includes  
3        (c) a third message that specifies a second address,  
4 wherein processing of the third message causes a value to  
5 be retrieved from a location in the first local storage  
6 that is associated with the second address and to be sent  
7 to the corresponding computer processor, and  
8        (d) a fourth message that specifies the second  
9 address, wherein processing of the fourth message prior to  
10 processing the third message guarantees that the value  
11 caused to be sent in processing the third message is a  
12 value that was previously stored in the memory system by  
13 one of the other processors.

1        11. The memory system of claim 9 further comprising:  
2        a main storage wherein values stored in the main  
3 storage are accessible to each of the plurality of local  
4 storages; and  
5        a controller configured to transfer data between the  
6 main storage and the plurality of local storages according  
7 to a plurality of stored rules.

1        12. The memory system of claim 11 wherein the  
2 plurality of stored rules includes:  
3        a rule for initiating a transfer of the first value  
4 from the local storages to the main storage after  
5 processing the first message and prior to processing the  
6 second message.



1        13. A computer processor for use in a multiple  
2 processor computer system in which the computer processor  
3 and one or more other computer processors are coupled to a  
4 storage system, the computer processor comprising:  
5        a storage capable of holding a sequence of  
6 instructions, wherein the sequence of instructions includes  
7 a first instruction that specifies a first address range  
8 and a second address range, and includes a first set of  
9 instructions that each specifies an address in the first  
10 address range and that are prior to the first instruction  
11 in the sequence, and a second set of instructions that each  
12 specifies an address in the second address range and that  
13 are after the first instruction in the sequence;  
14        an instruction scheduler coupled to said storage,  
15 wherein the instruction scheduler is configured to issue  
16 instructions in the sequence of instructions such that  
17 instructions in the second set of instructions do not issue  
18 prior to all of the instructions in the first set of  
19 instructions completing.

1        14. The computer processor of claim 13 wherein the  
2 first set of instructions includes instructions that may  
3 result in data previously stored in the storage system by  
4 one of the one or more other processors at an address in  
5 the first address range being transferred to the computer  
6 processor.

1        15. The computer processor of claim 14 wherein the  
2 second set of instructions includes instructions that each  
3 initiates a transfer of data from the computer processor to  
4 for storage at an address in the second address range such  
5 that the data is accessible to the one or more other  
6 processors.

1        16. The computer processor of claim 14 wherein the  
2 second set of instructions includes instructions that may  
3 result in data previously stored in the storage system by  
4 one of the one or more other processors at an address in  
5 the second address range being transferred to the computer  
6 processor.

1        17. The computer processor of claim 13 wherein the  
2 first set of instructions includes instructions that each  
3 completes after the instruction schedule receives a  
4 corresponding notification from the storage system that a  
5 value has been stored in the storage system at an address  
6 in the first address range such that the value is  
7 accessible to the one or more other processors.

1        18. The computer processor of claim 17 wherein the  
2 second set of instructions includes instructions that  
3 initiate a transfer of data from the computer processor to  
4 for storage at an address in the second address range such  
5 that the data is accessible to the one or more other  
6 processors.

1        19. The computer processor of claim 17 wherein the  
2 second set of instructions includes instructions that may  
3 result in data previously stored in the storage system by  
4 one of the one or more other processors at an address in  
5 the second address range being transferred to the computer  
6 processor.

1        20. A method for accessing a memory system from a  
2 processor in a multiple processor computer system,  
3 comprising:

4        (a) in a first processor that is coupled to a first  
5 local storage in the memory system, processing a first  
6 instruction that specifies a first address and a first  
7 value, including storing the first value at a location in  
8 the first local storage that is associated with the first  
9 address, and

10       (b) in the first processor, after processing the first  
11 instruction, processing a second instruction that specifies  
12 the first address, wherein processing of the second  
13 instruction completes after the first value is stored at a  
14 location in a shared storage in the memory system that is  
15 associated with the first address.

1           21. The method of claim 20 further comprising:  
2           (c) in a second processor that is coupled to a second  
3 local storage in the memory system, processing a third  
4 instruction that specifies the first address, including  
5 retrieving a value from a location in the second local  
6 storage that is associated with the first address, and  
7           (d) in the second processor, processing a fourth  
8 instruction that specifies the first address prior to  
9 processing the third instruction and after the first  
10 processor has completed processing the second instruction,  
11 including retrieving the first value from the location in  
12 the shared storage that is associated with the first  
13 address and storing the first value at a location in the  
14 second local storage that is associated with the first  
15 address, whereby the value retrieved in the processing of  
16 the third instruction is the first value, which was  
17 specified in the first instruction.

1        22. A method for providing data storage for a  
2 plurality of computer processors in a memory system that  
3 includes a plurality of local storages, including a first  
4 local storage unit and other local storage units, the  
5 method comprising:  
6        receiving at the first local storage a first message  
7 from a corresponding one of the plurality of computer  
8 processors, wherein the first message specifies a first  
9 address and a first value;  
10       processing the first message by the first local  
11 storage unit including storing the first value at a  
12 location in the local storage unit that is associated with  
13 the first address, such that, for at least a period of  
14 time, the other local storage units do not have access to  
15 the first value;  
16       receiving at the first local storage a second message  
17 from the corresponding one of the plurality of computer  
18 processors, wherein the second message specifies the first  
19 address;  
20       processing the second message by the first local  
21 storage unit after processing the first message such that  
22 the processing of the second message completes after the  
23 first value can be accessed by each of the other local  
24 storage units.

1        23.. The method of claim 22 further comprising:  
2        receiving by the first local storage unit a third  
3 message from the corresponding one of the plurality of  
4 computer processors, wherein the third message specifies a  
5 second address;  
6        processing the third message including retrieving a  
7 value from a location in the first local storage that is  
8 associated with the second address and sending the  
9 retrieved value to the corresponding one of the plurality  
10 of computer processors;  
11        receiving by the first local storage unit a fourth  
12 message from the corresponding one of the plurality of  
13 computer processors, wherein the fourth message specifies  
14 the second address; and  
15        processing of the fourth message prior to processing  
16 the third message;  
17        wherein the value sent in processing the third message  
18 is a value that was previously stored in the memory system  
19 by one of the other processors.

1        24. The method of claim 22 wherein the memory system  
2 includes a main storage wherein values stored in the main  
3 storage are accessible to each of the plurality of local  
4 storages, and the method further comprises:  
5        accessing a plurality of stored rules; and  
6        transferring data between the main storage and the  
7 plurality of local storages according to the accessed  
8 rules.

1        25. The method of claim 24 wherein transferring data  
2 between the main storage and the plurality of local  
3 storages includes initiating a transfer of the first value  
4 from the local storages to the main storage after  
5 processing the first message and prior to processing the  
6 second message.

1        26. A method for scheduling instructions in a  
2 computer processor, comprising:  
3        accepting a sequence of instructions that includes a  
4 first instruction that specifies a first address range and  
5 a second address range, a first set of instructions that  
6 each specifies an address in the first address range and  
7 that are prior to the first instruction in the sequence,  
8 and a second set of instructions that each specifies an  
9 address in the second address range and that are after the  
10 first instruction in the sequence;  
11        executing the first instruction, including waiting for  
12 all instructions in the first set to complete; and  
13        executing instructions in the second set only after  
14 executing the first instruction.